CLAIMS

1.   An apparatus in a pipeline microprocessor, for
     ensuring coherency of instructions within stages of
     the pipeline microprocessor, the apparatus comprising:

     instruction cache management logic, configured to
          receive an address corresponding to a next
          instruction, and configured to detect that a part
          of a memory page corresponding to said next
          instruction cannot be freely accessed without
          checking for coherency of the instructions within
          said part of said memory page and, upon
          detection, configured to provide said address;
          and

     synchronization logic, configured to receive said
          address from said instruction cache management
          logic, and configured to direct data cache
          management logic to check for coherency of the
          instructions within said part of said memory
          page, and, if the instructions are not coherent
          within said part of said memory page, said
          synchronization logic is configured to direct the
          pipeline microprocessor to stall a fetch of said
          next instruction until the stages of the pipeline
          microprocessor have executed all preceding
          instructions.

2. The apparatus as recited in claim 1, wherein said
    instruction cache management logic evaluates an
    instruction translation lookaside buffer (ITLB) entry
    corresponding to said address to detect that said part
    cannot be freely accessed.

3. The apparatus as recited in claim 2, wherein said ITLB
    entry corresponds to said memory page.

4. The apparatus as recited in claim 3, wherein said ITLB
    entry comprises a plurality of part-page ownership
    bits.

5. The apparatus as recited in claim 4, wherein one of
    said plurality of part-page ownership bits corresponds
    to said part of said memory page.

6. The apparatus as recited in claim 5, wherein remaining
    ones of said plurality of part-page ownership bits
    correspond to remaining parts of said memory page.

7. The apparatus as recited in claim 5, wherein said part
    can be freely accessed if said one of said plurality
    of part-page ownership bits is set.

8. The apparatus as recited in claim 5, wherein said part
    cannot be freely accessed if said one of said
    plurality of part-page ownership bits is not set.

9. The apparatus as recited in claim 4, wherein said
    plurality of part-page ownership bits comprise four
    part-page ownership bits, and wherein said part
    comprises one-quarter of said memory page.

10. The apparatus as recited in claim 1, wherein said data
     cache management logic evaluates a data translation
     lookaside buffer (DTLB) entry corresponding to said
     address to detect that the instructions are not
     coherent within said part of said memory page.

11. The apparatus as recited in claim 10, wherein said
     DTLB entry corresponds to said memory page.

12. The apparatus as recited in claim 11, wherein said
     DTLB entry comprises a plurality of part-page
     ownership bits.

13. The apparatus as recited in claim 12, wherein one of
     said plurality of part-page ownership bits corresponds
     to said part of said memory page.

14. The apparatus as recited in claim 13, wherein
     remaining ones of said plurality of part-page
     ownership bits correspond to remaining parts of said
     memory page.

15. The apparatus as recited in claim 13, wherein the
     instructions are not coherent within said part if said
     one of said plurality of part-page ownership bits is
     set.

16. The apparatus as recited in claim 13, wherein the
     instructions are coherent within said part if said one
     of said plurality of part-page ownership bits is not
     set.

17. An apparatus in a pipeline microprocessor, for
    ensuring coherency of instructions within stages of
    the pipeline microprocessor, the apparatus comprising:

    data cache management logic, configured to receive an
        address corresponding to a store instruction that
        is pending, and configured to detect that a part
        of a memory page corresponding to said store
        instruction cannot be freely accessed without
        checking for coherency of the instructions within
        said part of said memory page, and, upon
        detection, configured to provide said address;
        and

    synchronization logic, configured to receive said
        address from said data cache management logic,
        and configured to direct instruction cache
        management logic to check for coherency of the
        instructions within said part of said memory
        page, and, if the instructions are not coherent
        within said part of said memory page, said
        synchronization logic is configured to direct the
        pipeline microprocessor to flush preceding stages
        of the pipeline microprocessor.

18. The apparatus as recited in claim 17, wherein said
    data cache management logic evaluates a data
    translation lookaside buffer (DTLB) entry
    corresponding to said address to detect that said part
    of said memory page cannot be freely accessed.

19.   The apparatus as recited in claim 18, wherein said
      DTLB entry corresponds to said memory page.

20.   The apparatus as recited in claim 19, wherein said
      DTLB entry comprises a plurality of part-page
      ownership bits.

21.   The apparatus as recited in claim 20, wherein one of
      said plurality of part-page ownership bits corresponds
      to said part of said memory page.

22.   The apparatus as recited in claim 21, wherein
      remaining ones of said plurality of part-page
      ownership bits correspond to remaining parts of said
      memory page.

23.   The apparatus as recited in claim 21, wherein said
      part of said memory page can be freely accessed if
      said one of said plurality of part-page ownership bits
      is set.

24.   The apparatus as recited in claim 21, wherein said
      part of said memory page cannot be freely accessed if
      said one of said plurality of part-page ownership bits
      is not set.

25.   The apparatus as recited in claim 20, wherein said
      plurality of part-page ownership bits comprise four
      part-page ownership bits, and wherein said part
      comprises one-quarter of said memory page.

26. The apparatus as recited in claim 17, wherein said instruction cache management logic evaluates an instruction translation lookaside buffer (ITLB) entry corresponding to said address to detect that the instructions are not coherent within said part of said memory page.

27. The apparatus as recited in claim 26, wherein said ITLB entry corresponds to said memory page.

28. The apparatus as recited in claim 27, wherein said ITLB entry comprises a plurality of part-page ownership bits.

29. The apparatus as recited in claim 28, wherein one of said plurality of part-page ownership bits corresponds to said part of said memory page.

30. The apparatus as recited in claim 29, wherein remaining ones of said plurality of part-page ownership bits correspond to remaining parts of said memory page.

31. The apparatus as recited in claim 29, wherein the instructions are not coherent within said part if said one of said plurality of part-page ownership bits is set.

32. A method in a pipeline microprocessor, for ensuring coherency of instructions within stages of the pipeline microprocessor, the method comprising:

within a data cache, detecting that a part of a memory
page corresponding to a pending store instruction
cannot be freely accessed without checking for
coherency of the instructions within the part of
the memory page;

directing logic within an instruction cache to check
for coherency of the instructions within the part
of the memory; and

if the instructions are not coherent, flushing
preceding stages of the pipeline microprocessor.

33. The method as recited in claim 32, wherein said
detecting comprises:

evaluating a data translation lookaside buffer (DTLB)
entry corresponding to a target address for the
pending store instruction.

34. The method as recited in claim 33, wherein the DTLB
entry corresponds to the memory page.

35. The method as recited in claim 34, wherein the DTLB
entry comprises a plurality of part-page ownership
bits.

36. The method as recited in claim 35, wherein one of the
plurality of part-page ownership bits corresponds to
the part of the memory page.

37.   The method as recited in claim 36, wherein remaining ones of the plurality of part-page ownership bits correspond to remaining parts of the memory page.

38.   The method as recited in claim 37, wherein the part of said memory page can be freely accessed if the one of the plurality of part-page ownership bits is set.

39.   The method as recited in claim 37, wherein the part of the memory page cannot be freely accessed if the one of the plurality of part-page ownership bits is not set.

40.   The method as recited in claim 35, wherein the plurality of part-page ownership bits comprise four part-page ownership bits, and wherein the part comprises one-quarter of the memory page.

41.   The method as recited in claim 32, wherein said directing comprises:

      evaluating an instruction translation lookaside buffer (ITLB) entry corresponding to a target address for the pending store instruction.

42.   The method as recited in claim 41, wherein the ITLB entry corresponds to said memory page.

43.   The method as recited in claim 42, wherein the ITLB entry comprises a plurality of part-page ownership bits.

44. The method as recited in claim 43, wherein one of the plurality of part-page ownership bits corresponds to the part of the memory page.

45. The method as recited in claim 44, wherein remaining ones of the plurality of part-page ownership bits correspond to remaining parts of the memory page.

46. The method as recited in claim 45, wherein the instructions are not coherent within the part if the one of said plurality of part-page ownership bits is set.